X-2. PHASED-ARRAY DIGITAL TIME DELAY PHASER USING LATCHING FERRITE SWITCHES

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Introduction. Recent developments in latching ferrite phase shifters permit phase control within 360 degrees at microsecond switching times for phased-array antenna elements. When an array antenna must handle large instantaneous signal bandwidths, the simple modulo 2π phase control provided by these phase shifters must be supplemented by real time delays of several nanoseconds. The time delay phaser described below provides four-bit digital subdivision of an 8.7-nanosecond total time delay in increments of 0.58 nanosecond.

Principles of Operation. A functional diagram of the complete four-bit time delay unit (TDU) is shown in Figure 1. Two reversible waveguide circulators in each bit are used to switch to either of two alternate signal paths. In this circuit differential time delay is provided by different lengths of TEM transmission line in each signal path. The complete single-bit diagram in Figure 2 shows a nondispersive attenuator in the shorter path to balance the attenuation of the longer path and thus provide delay-independent signal amplitude. A circulator-isolator in each path virtually eliminates phase and amplitude errors due to internal reflections.

General Design. A photograph of the complete delay unit is shown in Figure 3, and an internal view of one bit is shown in Figure 4. The circulator switches, circulator-isolators, and attenuators are constructed in X_B-band waveguide. Each time delay bit consists of two aluminum assemblies containing machined waveguide circuitry and connected by two semi-rigid coaxial delay cables. The four bits are interconnected by short lengths of X_B-band waveguide. Input and output ports are designed with matching sections to allow low VSWR connection to standard X-band guide.

Circulator-Switch Design. A recently developed three-port latching junction switch is the key component in the time delay unit 1 . The switch functions as a symmetrical three-port junction circulator. The magnetic fields required for circulator operation are supplied entirely by remanent magnetization in the microwave ferrite material. To maximize the magnitude of the remanent fields, the ferrite member is made in a tri-toroidal shape and a ferrite material having a high remanence ratio, B_r/B_s, is used. A small wire enters through the side wall of the guide and passes through the holes in the ferrite to form a switching coil. The magnetization of the ferrite and the sense of circulation are reversed by passing a current pulse through the switching coil.

The circulator has a 1-GHz bandwidth with greater than 20-db isolation and less than 0.25-db insertion loss. It switches between states in less than two microseconds when driven with a switching pulse of 150 microjoules. The device can handle 1000 watts peak power and 10 watts average power with no increase in insertion loss and less than one degree change in insertion phase.

Design of Miscellaneous Component Parts. The isolator in each path of each delay bit consists of a latching circulator and a miniaturized volumetric termination. This circulator is permanently latched to permit transmission in the forward direction.

The attenuator in the short path is a small slab of dielectric material having both electric and magnetic losses. The loss versus frequency characteristics of the attenuator can be modified by locating the material at various distances from the side wall of the guide. The size and position of the material were chosen to match the insertion loss characteristic of the differential coaxial line length in each bit.

The transition from coaxial line to waveguide consists of a dielectric tube inside the guide into which the center conductor of the coax extends as a probe. Additional dielectric blocks in the guide improve the matched bandwidth of the transition.

Delay Unit Performance. The insertion loss and time delay error of the complete four-bit delay unit are shown in Figure 5. The curves in Figure 5(a) represent the maximum and minimum insertion loss obtained when the delay unit is switched through all 16 possible states. Loss variations at most frequencies are less than ± 0.1db for all possible states and the average loss varies less than ± 0.3 db across the 10 percent band from 8.4 to 9.3 GHz. The unit may be operated at peak input power levels up to 1.0 kw with no variation in insertion loss. At higher power levels, limiting occurs due to nonlinear losses in the ferrite.

Typical phase errors are shown in Figure 5(b). A broadband balanced waveguide phase bridge with one time delay unit in each arm is used in these measurements. To measure the phase error of one unit having a particular delay setting, the unit is switched to the desired setting and a calibrated length of coaxial delay cable is added to the opposite bridge arm. The resultant plot indicates the difference between actual and desired differential phase shift in the unit.

The input VSWR of the delay unit is determined primarily by the VSWR of the circulator-switch in the first bit and is less than 1.25:1 from 8.4 to 9.4 GHz. Differences in VSWR due to switching of the first bit are less than 1.08; differences due to switching of other bits are less than 1.02.

Conclusion. The real time delay phaser described herein demonstrates the feasibility of building medium power X-band time delay units with 5 degree accuracy, 10 percent bandwidth, microsecond switching speeds, and efficient latching operation. It is also evident that performance is largely determined by the ferrite switch and that increased bandwidth of this component will allow wider bandwidths and less frequency-sensitive insertion loss characteristics in a time delay phaser.

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1. Goodman, P. C., "A Latching Ferrite Junction Circulator For Phased Array Switching Applications," Digest of the 1965 G-MTT International Symposium, pp. 123-6.

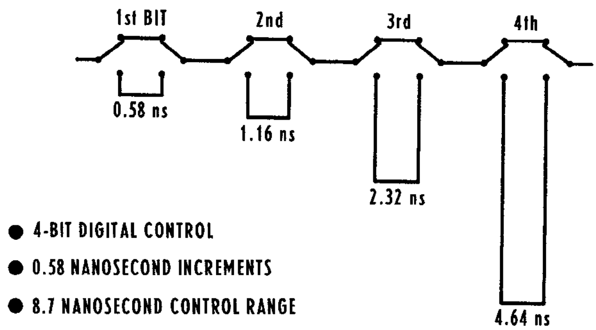

Figure 1. Functional Diagram of Four-Bit Time Delay Unit

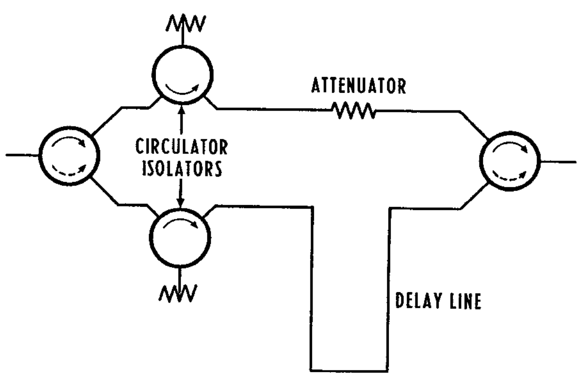

Figure 2. Diagram of Single-Bit Time Delay Network

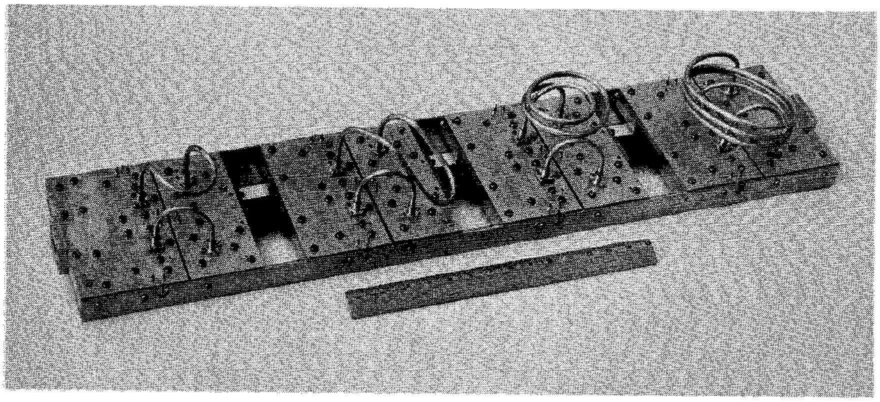

Figure 3. Complete Four-Bit Time Delay Unit

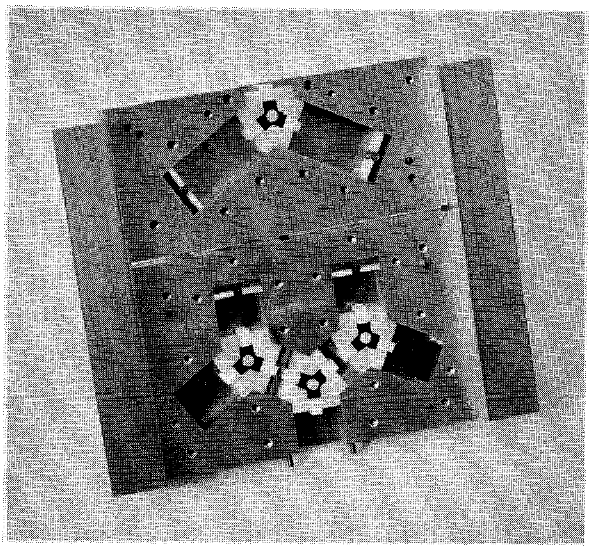

Figure 4. Internal View of Single Time-Delay Bit

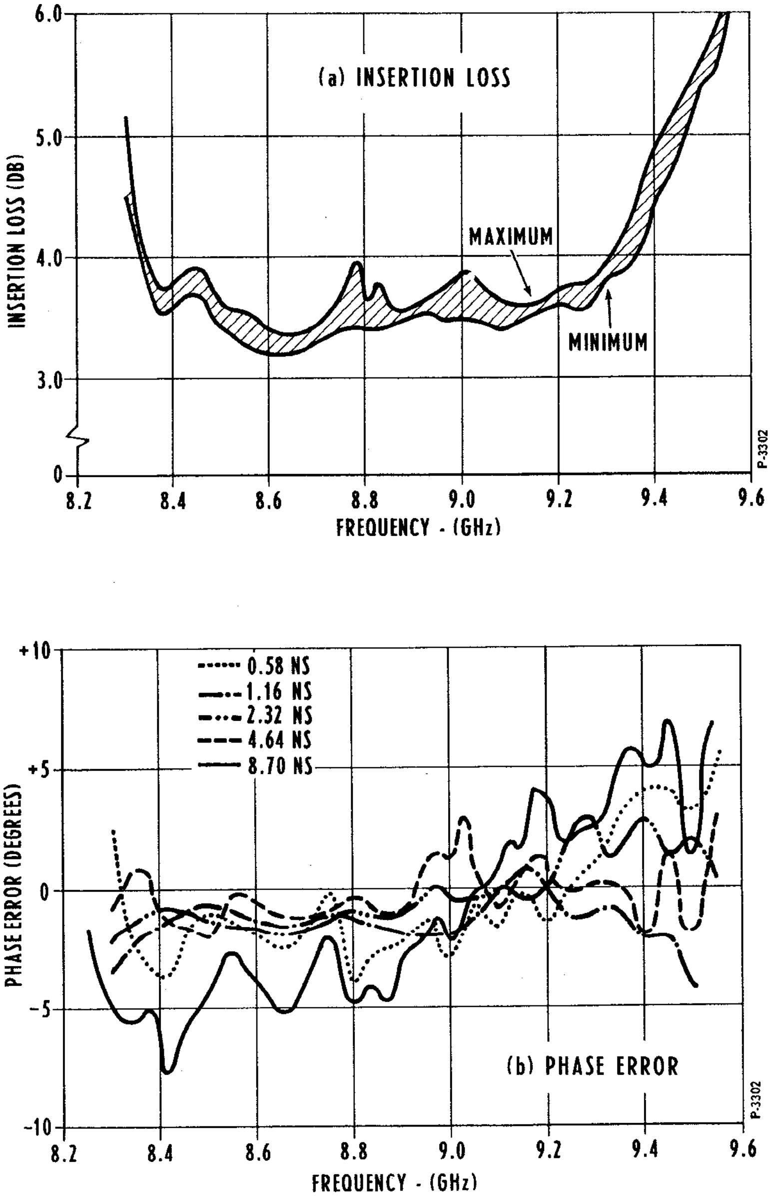

Figure 5. Delay Unit Operating Characteristics